



IEEE | **EMC**
SOCIETY

United Kingdom and Ireland Chapter

Co-Sponsored by



Hosted by

**UNIVERSITY OF
WESTMINSTER**

Design and SI/PI Analysis of High-Performance Memory Systems

Dr. Wendem Beyene; Analog & Mixed-Signal Architect, Facebook Inc

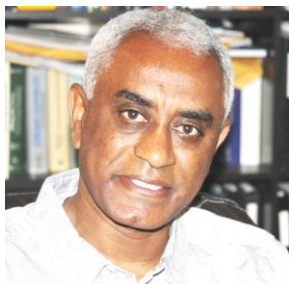
IEEE EMC Society Distinguished Lecturer

Monday 3rd October 2022, from 3pm

*C1.18 Pavilion, Cavendish Building, University of Westminster,
115 New Cavendish Street, London, W1W 6UW, United Kingdom*

Networking from 3pm, Presentation from 4pm

The presentation starts with an introduction to memory systems in computing devices such as computers, tablets or smartphones. Then, an in-depth analysis of standard memory systems for low-power and high-performance applications is provided. The interactions between the signaling, clocking architecture and packaging technology of a memory interface as well as how these interactions determine the achievable data rates and power efficiency are discussed. Signaling and clocking schemes for standard memories, including DDR3 and DDR4 (DDR5), and mobile memories, such as LPDDR3 and LPDDR4 (LPDDR5) are detailed and compared against each other. The emerging 2.5D/3D memory systems such as HBM1/2/2E, and HMC1/2 and beyond are also presented. Packaging options such as BGA, PoP, and the emerging 2.5D/3D are also discussed. To analyze and compare different state-of-the-art memory interfaces, the following metrics are used in the analysis: cost, power efficiency, bandwidth, design complexity, signal and power integrity, thermal solution, and form factor. The audience will gain an in-depth understanding of high-speed memory interfaces; learn about the interactions between the signaling, clocking architecture and packaging technology of a memory interface, and find out how those interactions determine the achievable data rates and power efficiency. The presentation will conclude by demonstrating how this knowledge can be used to analyze and compare different state-of-the-art memory interfaces to help attendees implement or select a solution which best fits their specific application.



Dr. Wendem T. Beyene was born in Addis Ababa, Ethiopia. He received the B.S. and M.S. degrees in electrical engineering from Columbia University, New York, NY, USA, in 1988 and 1991, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana-Champaign, USA, in 1997. In the past, he was employed by IBM, Hewlett-Packard, and Agilent Technologies. In 2000, he joined Rambus Inc., Los Altos, CA, USA, and was responsible for signal integrity of multi-gigabit parallel and serial interfaces. During 2017-2020 he worked at Intel and was responsible for signal and power integrity analysis of high-performance FPGA including fabric and high-speed I/O subsystems as well as I/O modeling. In 2020 he joined Facebook as an Analog & Mixed-Signal Architect in Meta Reality Lab. Dr. Beyene has authored or co-authored numerous refereed publications in various leading IEEE Transactions and conferences. These publications covered various disciplines including package and interconnect modeling, interface design and analysis as well as application of machine learning and optimization techniques to signal and power integrity of complex systems. He is currently a Senior Area Editor - Electrical Performance of Integrated Systems of IEEE Trans. On CPMT and is a Senior Member of Institute of Electrical and Electronic Engineers (IEEE). He also serves on several leading technical program committees, including EPEPS and DTMES.

This presentation is free to attend, and open to all, whether you are an IEEE member, EMC Society member, or not. Advance registration is not required, but it would aid in our planning if you can indicate if you plan to attend by visiting;

<https://events.vtools.ieee.org/m/323489>